WHAT IS CLAIMED IS:

1. A communication control apparatus for collecting cells belonging to a same connection among a plurality of cells which are inputted, assembling a frame every connection, and outputting each of said frames as frame data, comprising:

a frame assembly memory having a plurality of areas which were set so as to correspond to a maximum one of a plurality of frame lengths which are handled;

a memory write control unit constructed in a manner such that when a cell of a new connection is inputted, said new connection is allocated to said empty area in said frame assembly memory to which the connection is not allocated yet and said cell is written therein, and on the other hand, when the cell of the same connection as the connection which has already been allocated to any of said areas is inputted, said cell is written into said area to which said connection has already been allocated, and if the cells of one frame have already been written in said area, said connection is allocated to another new area, and said input cell is written therein; and

a memory read control unit which reads out said collected cells of one frame from said frame assembly memory and outputs them as completed-frame data.

2. An apparatus according to claim 1, wherein each time the cell of the same connection is inputted, said memory write control unit executes an arithmetic operation for discriminating validity of data including said cell stored in said area in which said cell is written.

3. An apparatus according to claim 1, wherein when there is an error of validity of the data of one frame stored in said area, said memory write control unit abandons said frame.

4. An apparatus according to claim 3, wherein when the cells of one frame are written into said area, said memory write control unit abandons said frame.

5. An apparatus according to claim 2, wherein the arithmetic operation for discriminating the validity of said data is a CRC logical arithmetic operation regarding a payload of each cell.

6. An apparatus according to claim 2, wherein the arithmetic operation for discriminating the validity of said data is a parity check logical arithmetic operation regarding a payload of each cell.

7. An apparatus according to claim 2, wherein the arithmetic operation is an OR arithmetic operation of a Loss Priority bit regarding a header of each cell.

8. An apparatus according to claim 2, wherein the arithmetic operation is an AND arithmetic operation of a Loss Priority bit regarding a header of each cell.

9. An apparatus according to claim 1, wherein each time the cell of the same connection is inputted, said memory write control unit executes a logical arithmetic operation of data up to said cell in one frame of said connection, outputs a result of said logical arithmetic operation until the last

cell at a point of time when the cells of one frame have been written, and discriminates validity of said frame on the basis of the result of said logical arithmetic operation of each cell constructing said frame on the basis of said output result.

10. An apparatus according to claim 1, wherein each time the cell of the same connection is inputted, said memory write control unit measures an arrival interval in a range from an input of the cell that was inputted at timing of one cell before said input cell to an arrival of the subsequent input cell with respect to said connection, and abandons said frame in said area regarding said connection of said cell if said arrival interval exceeds a predetermined value.

11. An apparatus according to claim 2, wherein each time the cell of the same connection is inputted, said memory write control unit measures an arrival interval in a range from an input of the cell that was inputted at timing of one cell before said input cell to an arrival of the subsequent input cell with respect to said connection, and abandons said frame in said area regarding said connection of said cell if said arrival interval exceeds a predetermined value.

12. An apparatus according to claim 1, wherein said memory write control unit measures an arrival interval in a range from an input of the first cell belonging to the frame of the same connection to an input of the last cell belonging to said frame, and abandons said frame when said arrival interval exceeds a predetermined value.

13. An apparatus according to claim 2, wherein said memory write control unit measures an arrival interval in a range from an input of the first cell belonging to the frame of the same connection to an input of the last cell belonging to said frame, and abandons said frame when said arrival interval exceeds a predetermined value.